

Robert Bao

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EDUCATION

University of Illinois Urbana-Champaign

*MS/PhD in ECE (Advised by Prof. Rakesh Kumar), **Promise of Excellence Fellowship*** Aug. 2024 – May 2026/29

*Bachelor of Science in Computer Engineering, **Highest Honors, IEEE-HKN, GPA: 3.95/4.0*** Aug. 2021 – May 2024

- Computer Architecture, VLSI System Design, Operating Systems, Digital Systems, Data Structures/Algorithms

SKILLS

Software: C/C++, Python, Bash, Assembly, Git, Unix

Hardware: Verilog/SystemVerilog, Quartus, Vivado, RISC-V, Synopsys (Verdi, DesignVision), I2C, SPI, Cadence Virtuoso

EXPERIENCE

IBM | Sr. Pre-Silicon Verification Intern

May 2024 – Aug. 2024

- Modernized mission-critical verification tooling to work with an internal file system migration
- Identified errors in tracing tools and hardware defects by leveraging system simulation models run on AWAN accelerators
- Developed RISC-V tracing panel for internal waveform viewer to expedite viewing signals of interest

IBM | Processor Logic Design Intern

May 2023 – Aug. 2023

- Contributed to development of future Z CPUs by developing new branch prediction architectures for future Power and Z processors, discovering 15% IPC improvements for target workloads
- Integrated separate Power and Z branch prediction models into one standardized model for streamlined data analysis
- Automated simulation runs and data analysis from benchmarks and tuned branch prediction structure parameters to optimize IPC

ECE Department at UIUC | Course Assistant for ECE 110/210/220/385

Jan. 2022 – May 2024

- Taught lab curriculum for Intro to Electronics, Signal Processing, Computer Systems, and Digital Systems
- Guided students through circuit building, using lab equipment (oscilloscope, signal generator, spectrum analyzer, etc.), C programming, and SystemVerilog designs using Vivado

Healthcare Engineering Systems Center at UIUC | Research Assistant

Mar. 2023 – May 2023

- Built clinical breast examination training simulator by using Arduino to collect and send data in real time from a force sensing array to server via MQTT protocol
- Created augmented reality app using Vuforia in Unity to fetch and display force data on a virtual phantom

Google | Computer Science Summer Institute Scholar

July 2021 – Aug. 2021

- Exceeded expectations in 10 individual coding projects in JavaScript by using concepts such as object oriented programming, variables, data types, and functions
- Delivered a collaborative final project presentation that included a live demonstration to Google employees

PROJECTS

Basic Macro Devices RISC-V CPU

Mar. 2024 – May 2024

- Built a 2-way superscalar Out-Of-Order RISC-V CPU using explicit register renaming supporting RISC-V(IM) ISA
- Features include Dadda multiplier, Synopsys IP divider, BTB & BHT/GShare tournament branch predictor, 4-way set-associative PLRU pipelined caches with next-line prefetcher
- Verified design using random coverage, targeted testing with Synopsys VCS and Verdi, Spike

32-Bit RISC-V Datapath

Mar. 2024

- Created (from scratch) schematic and layout for a RISC-V CPU Datapath including register file, ALU, barrel shifter
- Used bit-sliced design to maximize reusability and minimize area consumption

Linux-Like OS

Dec. 2023

- Collaborated within a three person team to build a Linux-like operating system from scratch including global descriptor table, interrupt descriptor table, paging, file system, system calls, interrupts, and several hardware drivers (RTC, keyboard, PIC, PIT, terminal)
- Implemented multiple terminal screens and round-robin scheduling

Object-tracking Camera & Sensor Suite

Dec. 2023

- Programmed I2C and SPI protocols from scratch, developed in Verilog on OpalKelly XEM7310 development board
- Utilized block-throttled pipe communications to achieve over 20 frames per second from onboard camera while also collecting data from magnetometer and accelerometer
- Interfaced FPGA with Python/OpenCV for image processing and thresholding to control a PWM motor for tracking